REMARKS

This Amendment is filed in response to the Office Action dated January 28, 2002. Applicant first notes with appreciation the Examiner's thorough examination of the application as evidenced by the Office Action. In response to the Office Action, Applicant has amended independent Claim 1 to clear up informalities noted by the Office Action. As discussed in detail below, Applicant respectfully submits that amended independent Claim 1, as well as the claims that depend therefrom include recitations that patentably define over the cited references, taken either individually or in combination. In light of this, Applicant respectfully requests reconsideration and allowance of the application.

I. Consideration Of Previously Submitted Information Disclosure Statement

It is noted that an initialed copy of the PTO Form 1449 that was submitted with Applicant's Information Disclosure Statement filed October 22, 2001 has not been returned to Applicant's representative with the Office Action. Accordingly, it is requested that an initialed copy of the Form 1449 be forwarded to the undersigned with the next communication from the PTO. In order to facilitate review of the references by the Examiner, a copy of the Information Disclosure Statement and the Form 1449 are attached hereto. Copies of the cited references were provided at the time of filling the original Information Disclosure Statement, and, therefore, no additional copies of the references are submitted herewith. Applicant will be pleased to provide additional copies of the references upon the Examiner's request if it proves difficult to locate the original references.

II. Objected Claim 1 Is Now In Compliance

In paragraph 6, the Office Action objects to Claim 1 for containing certain informalities. Specifically, the Office Action objects to the phrase "at least one copybus to be connected to said at least one port . . .." The Office Action recommends the following amendments, which have been accepted by the Applicant and implemented in this Amendment with minor changes "copybus [to be] connected to <u>each of</u> said at least one <u>ports having</u> [port with] the copybus-

function." Applicant submits that these amendments to independent Claim 1 overcome the objections noted in the Office Action.

III. The Rejections

In paragraphs 9-14, the Office Action rejects all of the pending claims of the application. In particular, the Office Action rejects Claims 1 and 3 under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,321,298 to Hubis. The Office Action alleges that the Hubis '298 patent discloses a shared memory having a plurality of memories accessible from a copybus side and a user side, at least one copybus, where the shared memory copies writes to one of the memories to the other memories through the copybus. The Office Action acknowledges that the Hubis '298 patent may be interpreted as not disclosing multi-port memory devices. For this reason, the Office Action also rejects the claims under 35 U.S.C. § 103(a) as obvious in light of the combination of the Hubis '298 patent with either U.S. Patent No. 6,223,260 to Gujral et al. or U.S. Patent No. 6,021,472 to Hamaguchi. This Office Action alleges that these references disclose multi-port memories and that it would be obvious to combine them with the Hubis '298 patent. Applicants respectfully disagree with these rejections as they apply to amended independent Claim 1.

IV. The Claims Are Patentable

Applicant respectfully submits that amended independent Claim 1, as well as the claims that depend therefrom, is patentable over the cited references taken either individually or in combination. More specifically, Applicant submits that none of the cited references individually or in combination teaches or suggests a shared memory having true multi-port memories with N ports capable of N concurrent accesses, as recited in amended independent Claim 1.

Applicant first submits that the Hubis '298 patent does not teach or suggest anywhere in its disclosure the use of multi-port memories. On this point, the Office Action alternatively argues that controllers may be considered part of the cache as discussed in the Gujral '260 and Hamaguchi '472 patents to thereby form 2-port memories. Applicants argue, however, that such

a combination forms a *pseudo 2-port memory* (defined later) not a multi-port memory. Pseudo 2-port memories have the technical disadvantage of allowing only access bandwidth of a 1-port memory, not bandwidth of 2 ports, (i.e., not bandwidth N for N ports as recited in the claims). The functional reason for the controller in the Gujral '260 and Hamaguchi '472 patents is to transform concurrent accesses of the memory from 2 external ports into internally sequential accesses, not concurrent accesses, as with a *true multi-port memory*. Consequently, the pseudo 2-port memory of the Gujral '260 and Hamaguchi '472 patents cannot be used in an application requiring access bandwidth of 2 ports, but instead, can only be used for applications with an average access bandwidth equal to or smaller than 1.

The following definitions may be helpful in understanding this aspect:

1. Shared Memory - is defined as a memory capable of supplying an identical data base to several users, i.e., sharing the possibility of read and write accesses to the identical data base by all of the users.
2. True Multi-port Memory - a memory having N external independent ports that allow internal concurrent accesses from all N ports.
3. Pseudo Multi-port Memory - a memory having N external independent ports but allows internally concurrent access from k ports, where k is smaller than N.

The important advantage of a true multi-port memory over a pseudo multi-port memory is a higher access bandwidth by approximately a factor N/k. In the case that the number k is small in comparison to N, this advantage is very substantial. A pseudo multi-port memory provides interconnections for N port, but can be used only in systems where the average access bandwidth to the memory is less than N. This means that actual accesses from each port may occur only sporadically. However, for a system that really requires access to all N ports concurrently, a true multi-port memory, such as the one claimed in amended independent Claim 1, is required.

The main difference between the claimed invention and the Hubis '298 patent is that the claimed invention provides a shared memory having true multi-port memories. The Hubis '298

patent does not provide a shared memory based on true multi-port memories. In fact, it does not even disclose a shared memory based on pseudo multi-port memory. Rather, as displayed in Figure 3 of the Hubis '298 patent, shared storage devices (hard disks 108) and a method (backed disk bus 110, raid controllers 104j) for providing coherency of the 1-port cache systems (memory 202) of several processors connected to these shared hard disk are disclosed. This is not a shared memory having true multi-port memories as recited in amended independent Claim 1. In reality, the memory configuration of the Hubis '298 patent does not provide a shared memory because each of the caches contains, in general, different data. Since identical data may of course also be present in some of the caches, a method for cache coherency is needed and the aim of the Hubis '298 patent is to provide such a method. The purpose of the caches is just the usual purpose of caches, namely to buffer some data from the disk-based shared memory, which the corresponding processor is presently using.

As mentioned previously and reiterated here, the combination of the Gujral '260 and Hamaguchi '472 patents with the Hubis '296 patent does not teach or suggest a shared memory having true multi-port memories. Specifically, the Gujral '260 and Hamaguchi '472 patents do not disclose true multi-port memories. Instead, they disclose only pseudo multi-port memories. They include controllers, (which a true multi-port memory would not have), to turn concurrent reads of the two ports into sequential reads. As such, the pseudo multi-port memories support k concurrent accesses to an N port memory, while the true multi-port memory of the claimed invention provides N concurrent accesses to N ports.

In light of the above, Applicant respectfully submits that none of the cited references, taken either individually or in combination, teaches or suggests a shared memory having true multi-port memories as recited in amended independent Claim 1. As such, Applicant respectfully submits that amended independent Claim 1, as well as the claims that depend therefrom, is patentable over the cited references.

CONCLUSION

In view of the amended claim and the remarks presented above, it is respectfully submitted that all of the present claims of the application are in condition for immediate allowance. It is therefore respectfully requested that a Notice of Allowance be issued. The Examiner is encouraged to contact Applicant's undersigned attorney to resolve any remaining issues in order to expedite examination of the present application.

It is not believed that extensions of time or fees for net addition of claims are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 CFR § 1.136(a), and any fee required therefore (including fees for net addition of claims) is hereby authorized to be charged to Deposit Account No. 16-0605.

Respectfully submitted,

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I hereby certify that this paper is being facsimile transmitted to the Patent and Trademark Office at Fax No. 703-746-7239 on the date shown below. W. Kevin Ransom (Type or print name of person signing certification.) Signature 4/29/02 Date	I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231, on April 29, 2002. W. Kevin Ransom

Version with Markings to Show Changes Made:

In The Claims:

Please amend Claim 1 as follows:

1. A shared memory comprising:

a plurality of true multi-port memories having N independent ports that allow internal concurrent accesses of the memory for all N port, wherein each memory has [each having] at least one port with a copybus-function, and at least one port accessible from user side; and

at least one copybus [to be] connected to each of said at least one ports having [port with] the copybus-function;

wherein said shared memory is adapted to copy contents of one of said multi-port memories, which has been changed by a writing operation from said user side, to other multi-port memories through said at least one copybus.

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